Applicants' description of the prior art on page 5, line 21 to page 6, line 2, states:

> As shown in Fig. 1d, circuit patterns are formed on the copper stack plate 101 by a circuit pattern forming method such as an etching method. A circuit layer 106 obtained by the above-described process serves as circuit layers 106a, 106b and 106c of a multi-layer printed circuit board manufactured by a parallel or a batch stacking method, as shown in Fig. 3.

Therefore, applicants describe the prior art forms the circuit patterns on both sides of the outermost layers 106a and 106c before stacking takes place, as shown in FIGURE 3. If the circuit patterns are formed on layers 106a and 106c before pressing, circuit layers cannot be formed again after pressing. The Examiner states that pressing the double-sided layers 106a and 106c results in forming circuit patterns, and therefore, step (E) of Claim 1 is met. However, this interpretation clearly contradicts the specification that states that the circuit patterns are already formed on layers 106a and 106c before they are stacked and pressed. Therefore, the Examiner is not correct that stacking the layers 106a and 106c amounts to *forming* circuit patterns.

The Examiner states that limitations cannot be read into the claims. The Examiner states that the word "only" is being read into the claim. However, applicants are not reading limitations into the claims. The word "only" would be superfluous in Claim 1. Claim 1 states, "forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers." Claim 1 means that circuit patterns are formed, such as by etchings on the outermost layers after the board is pressed. This is evident from the claim language. As an example, FIGURE 9 shows that the outermost layers 506b and 506c are lacking circuit patterns on the outermost sides of each of the layers 506b and 506c. In FIGURE 10, the circuit patterns are formed on the outermost layers 506b and 506c of the pressed board.

In direct contrast to Claim 1, the outermost layers described as being prior art in FIGURE 3 already have circuit patterns formed on both sides of the outermost layers 106a

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and 106c. Therefore, in applicants' description of the prior art, the circuit patterns are not formed on the outermost layers of a board which is obtained by pressing the circuit layers and the insulating layers.

Accordingly, for at least the reasons provided above, applicants have not admitted to the method of Claim 1 being prior art. Furthermore, Claims 4, 5, 7, and 9 are dependent from Claim 1; therefore, these claims are also not anticipated.

Therefore, applicants respectfully request withdrawal of the rejection of Claims 1, 4, 5, 7, and 9.

The Rejection of Claims 1, 3-5, 7-10, and 14-17 Under 35 U.S.C. § 102(e).

Claims 1, 3-5, 7-10, and 14-17 are rejected under 35 U.S.C. § 102(e) as being anticipated by Kim et al. (U.S. Publication No. 2004/0194303). Applicants respectfully traverse the rejection. For a reference to be anticipatory, the reference must exactly describe the claimed invention.

Claim 16 recites, "pressing the circuit layers and insulating layers and filling the via holes of the circuit layers with the conductive paste from the via holes of the insulating layers to electrically connect the insulating layers with the circuit layers." The Examiner states that Kim et al. teaches omitting conductive paste from via holes. The Examiner also states that pressing the arranged circuit layers with the emptied via holes and the insulating layers having conductive paste would fill the emptied via holes in the circuit layers with conductive paste from the insulating layers to electrically connect the insulating layers with the circuit layers. The Examiner is making an assumption and is merely speculating. The Examiner cannot recite a passage in Kim et al. that teaches Claim 16 exactly. The Examiner appears to be relying on inherency.

"The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic." *In re Rijckaert*, 9 F.3d, 1531, 1534, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2112. IV. p.2100-57, rev. 3, August 2005.

Furthermore, in direct contrast with Claim 16, Kim et al. teaches that the via holes are not filled with conductive paste, but are plugged with copper. Kim et al. teaches, "[t]hereby, plated layers 305 are formed on both sides of the copper clad laminate 301, and the via holes 304 are plugged by copper." (Para. [0069].) In Figures 3B and 3D, Kim et al. teaches the via holes 304 are plugged by copper 305, not by conductive paste.

Claim 1 recites in step (E), "forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers."

Claims 14 and 15 each recite in step (E), "thereafter, forming circuit patterns on the outermost layers of a board obtained by pressing the circuit layers and the insulating layers."

At page 5, paragraph [0101], Kim et al. states: "the multi-layered PCB according to the present invention is structured such that a plurality of double-sided PCBs are continuously layered while insulating layers are inserted between the double-sided PCBs." Figure 7 of Kim et al. shows the uppermost circuit layer 306a, and the lowermost circuit layer 306c having a circuit pattern already formed on both sides of the layer before the pressing step. Therefore, the circuit patterns on layers 306a and 306c are not formed on the board which is obtained by pressing.

Accordingly, Claims 1, 14, 15, and 16 are not anticipated by Kim et al. Furthermore, Claims 3-5 and 7-10 depend directly from Claim 1, and Claim 17 depends from Claim 16; therefore, Claims 3-5, 7-10, and 16 are also not anticipated by Kim et al.

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CONCLUSION

In view of the foregoing remarks, applicants respectfully submit that all claims are allowable. If the Examiner has any further questions or comments, the Examiner may contact the applicants' attorney at the number provided below.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service in a sealed envelope as first class mail with postage thereon fully prepaid and addressed to Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the below date.

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